Gate Driver With Feed Forward Control of Turn off Performances of an IGBT in Short Circuit Conditions

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Abstract

This paper presents a short overview of an IGBT short circuit failure due to over-voltage, and discusses some protection methods. Every new generation of high power IGBT becomes faster and faster, with the collector current fall time of less than 100 ns, sometimes even 50 ns. Fast switching of the collector current, especially at current of 200 A or more, introduces a problem of turn off over-voltage. In case of overload or short circuit, the peak voltage on IGBT may exceed the break down voltage. As a result, the device can catastrophically fail in several tens of nanoseconds after collapse of the collector emitter voltage. To prevent a catastrophic failure, an advanced gate drive circuit has to be used instead of a standard gate drive with pure resistive gate control. A novel IGBT gate driver based on feed-forward control of the collector current slope and the collector emitter over-voltage in short circuit conditions is presented in this paper.

Introduction

Insulated Gate Bipolar Transistor (IGBT) modules are widely used in power converters such as PWM inverters in UPS and motor drives applications. These converters employed IGBT modules as active switches that operate in hard switching conditions. The IGBT gate driver is a key linking element between the logic control and the IGBT. In the gate driver design, we have to trade-off switching losses and turn-off delay time versus turn off over-voltages. The turn off over-voltage is a result of re-distribution of magnetic energy stored in the commutation inductance whenever the current flows through the IGBT module, the bus interconnection structure and bulky dc capacitors. Whenever the IGBT turns off, the energy stored in the commutation inductance is realized as a voltage spike. Even using carefully designed low inductive dc bus structure and low inductive bulky capacitors, the over-voltage is present. The total voltage across collector emitter chip can reach breakdown voltage (V_{CEBR}). It causes damage and, therefore reduction of the device life time. In the worst case, exceeding the RBSOA causes avalanche and catastrophic failure of the device.
A particular problem we will analyze in this paper is switch off of short circuit current. In such a case the collector current is several times of the device nominal current. Thus, the avalanche in short circuit is fatal and the IGBT fails catastrophically. This paper describes short circuit failure due to the commutation over-voltage, the generation mechanism and disadvantages of widely used protection circuits. In the second part of the paper, we present a novel feed-forward control of the IGBT over-voltage generated during a short circuit turn off. A possibility to control over voltage using a feed forward gate driver is presented and experimentally verified. The results are presented and shortly discussed in the paper.

The IGBT in short circuit

Power converters, especially variable speed drive converters, are very often exposed to a low impedance short circuit across the IGBT output terminals. It could be due to breakdown of the motor winding or motor cable insulation, manipulation error, or an error in the gate drive command. We may distinguish two different types of short circuit [23]. Typical waveforms of these two kinds of short circuit are depicted in Fig. 1.

The first type of short circuit is so-called hard short circuit or an arm short circuit. It is a short circuit with very low impedance, which appears while the IGBT is turned off. Afterward, the IGBT is turned on and the collector current rises steeply. The collector current rate is defined by the gate driver characteristics and the IGBT trans-conductance. The collector emitter voltage drops shortly and then again increases toward the dc bus voltage. In steady state, after the transients have been finished, the collector emitter voltage slightly differs from the dc bus voltage.

The second type of short circuit is depicted in Fig. 1b. The IGBT is already turned on. Afterward a short circuit appears, and the collector current rises with a rate defined by the short circuit impedance and the dc bus voltage. Once the current reaches the level defined by the trans-conductance and gate emitter voltage, the IGBT de-saturates, and the collector emitter voltage increases. At same time the gate emitter voltage begins to rise due to the Miller's capacitance displacement current and pumping effect of the gate emitter capacitance. The increase in the gate emitter voltage causes the collector current to increase too. It reflects as a large over-shoot in the collector current [2], which may lead to the IGBT letch up and catastrophic failure.

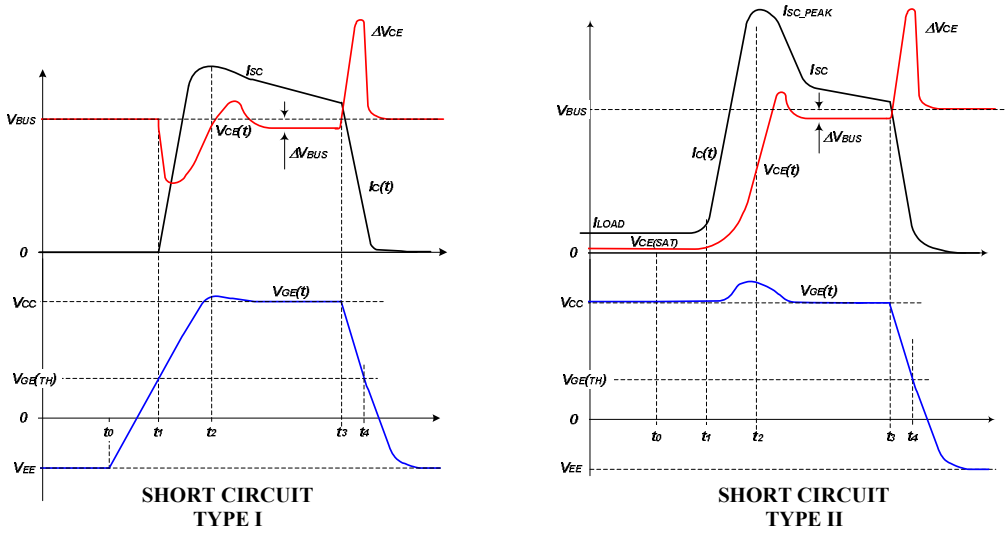

Fig. 1: Two types of short circuit.

Short circuit failure mechanisms

We can distinguish three different failure modes; exceeding the thermal limit of silicon, the collector emitter over-voltage failure and the IGBT letch up failure. In background, all these three failure modes are related to thermal stress and failure of silicon, the metallization or the bond wires of the device. Hereafter, we will shortly explain these failure modes.

- The thermal limit

In hard short circuit, the device sustains the entire dc bus voltage, while the collector current is several times of the device nominal current. The large amount of energy is realized on the IGBT chip. The IGBT junction temperature elevates steeply [16]. If the temperature exceeds the critical level, the device loses blocking capability due to thermal multiplication [1], [2]. The collector emitter voltage collapses quickly fallowed by the chip total destruction. The IGBT manufactures guarantee the short circuit time of 10 μs at specified conditions [22], [23].

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- The over-voltage failure

Such a kind of failure occurs if the collector emitter voltage exceeds the specified limit. The device fails in avalanche, and then entire collector current, which equals to the short circuit current, is focused in very narrow region of the silicon. The current density is enormous, resulting in localized high temperature spots. Hence, the device loses the blocking capability and the device voltage collapses in several tens of nanoseconds. To avoid such a failure, the commutation inductance has to be as low as possible [6], [7], [8], and an appropriate gate driver with the collector emitter voltage control should be used [10]. This failure mode would be considered in this paper and a new gate driver would be proposed.

- Letch up failure

An IGBT is a four layer structure having PNP and a parasitic NPN bipolar junction transistor connected in regenerative structure [2]. Normally, the NPN base-emitter junction is bypassed by diffusion resistance, and the base emitter voltage is far below 0.6V. Hence, the parasitic thyristor structure is disabled. In case of very high collector current, such as the short circuit current, the base emitter voltage may exceed 0.6V, and the parasitic thyristor will turn on. In such a case, there is not way to turn the device off by the gate command. Afterward, the device fails catastrophically due to enormous current and the energy dissipated on the chip, metallization and bond wires.

The IGBT model

For the further analysis we will briefly describe a simple linear model of the IGBT which operates in short circuit conditions. The steady state would be considered. The collector emitter voltage in steady state depends on short circuit resistance R_{SC} and magnitude of the short circuit current (1).

$$V_{CE} = V_{BUS} - R_{SC} I_{SC} = V_{BUS} - \Delta V_{BUS} . \quad (1)$$

As the collector emitter voltage is high, the internal MOSFET is in the active region. In this operational mode the total collector current of the IGBT strongly depends on the gate emitter voltage $\boldsymbol{V_{GE}}$, and slightly depends on the collector emitter voltage $\boldsymbol{V_{CE}}$. For simplicity of the analysis, we will neglect the plasma and space charge reaction time and consider that the IGBT operates in quasi steady state [2]. Then, the steady state equations will be used to define the collector current as a function on the gate emitter and collector emitter voltages, and the IGBT parameters.

$$I_C = K_m \cdot \left(\left(V_{GE} - V_{GE(TH)}\right)\left(\left(a_0 + a_1 V_{GE} + a_2 V_{GE}^2\right)\cdot V_{CE} - V_D\right) - \frac{\left(\left(a_0 + a_1 V_{GE} + a_2 V_{GE}^2\right)_1 \cdot V_{CE} - V_D\right)^2}{2} \right) \quad (2)$$

for $V_{CE} < V_{GE} + V_D - V_{GETH}$ and

$$I_C = K_m \cdot \left(V_{GE} - V_{GE(TH)}\right)^2 \text{ for } V_{CE} \geq V_{GE} + V_D - V_{GE(TH)} . \quad (3)$$

Where Km, a_0, a_1, and a_2 are coefficients depend on the device technology, $\boldsymbol{V_D}$ is the emitter base junction voltage, and $\boldsymbol{V_{GE(TH)}}$ is the gate emitter threshold voltage [1] and [2]. Equation (3) is further simplified and now we may expressed the collector current and its rate as

$$I_C \cong g_m \left(V_{GE} - V_{GE(TH)}\right) \quad \text{and} \quad \frac{dI_C}{dt} \cong g_m \frac{dV_{GE}}{dt} \quad (4)$$

where $g_m = \dfrac{\partial I_C}{\partial V_{GE}}$ is the IGBT forward trans-conductance.

In steady state the gate emitter voltage remains constant and equals to the positive gate voltage supply $\boldsymbol{V_{GE\_ON}}$. Thus, the steady state short circuit current is

$$I_{SC} \cong g_m \left(V_{GE\_ON} - V_{GE(TH)}\right). \quad (5)$$

Based on equation (4), we can develop an equivalent circuit of the IGBT in short circuit, given in Fig. 2. The voltage denoted as $\boldsymbol{V_{GE}}$ is the gate emitter voltage across the gate emitter connections on the chip level. This voltage significantly differs from the voltage across the external gate-emitter terminals due to the module internal inductances. The inductances $\boldsymbol{L_{EI}}$ and $\boldsymbol{L_E}$ represent the inductance of the bond wires and the module internal connections, respectively.

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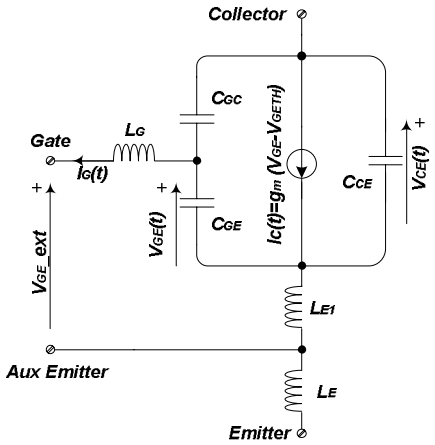

Fig. 2: Simplified equivalent model of an IGBT.

Turn off over-voltage

In this section we will briefly explain the IGBT turn off over-voltage generation mechanism. An equivalent circuit diagram we will use for the analysis is given in Fig. 3. Let's consider that the IGBT is fully conducting. Afterward, the gate emitter voltage is removed and commutation begins. While the IGBT is turning off, the collector current is commuting to the free wheeling diode (FWD). The commutation current rate is defined by the IGBT physic and the gate drive characteristics.

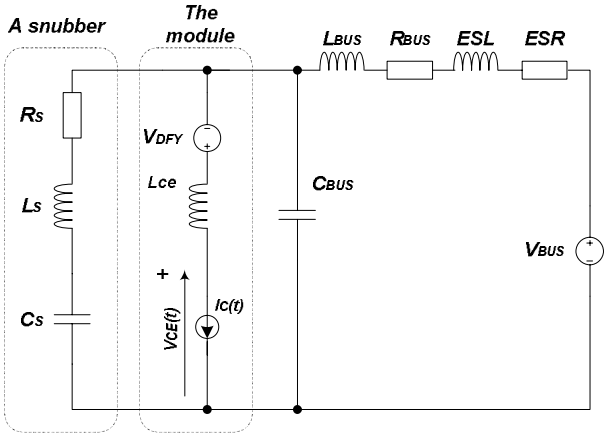

Fig. 3: Simplified commutation circuit of an inverter leg.

Switching of the IGBT generates over-voltage due to re-distribution of the magnetic energy stored in the commutation inductance. Referring to the equivalent circuit diagram given in Fig. 3, the total collector emitter voltage during turn off can be defined as

$$V_{CE} = V_{BUS} + \left(L_{BUS} + ESL_E + L_{CE}\right)\left|\frac{dI_C}{dt}\right| \cdot k_S + V_{DFDY}\,, \tag{6}$$

where L_{BUS} is equivalent inductance of the bus structure; ESL_E is equivalent inductance of the bus (electrolytic) capacitor; L_{CE} is the stray inductance of the IGBT module; and V_{DFDY} is forward recovery voltage of FWD, typically 10 to 50 V [23].

The coefficient k_S=1.1 to 1.5 takes in the account an overshoot due to the parasitic capacitance of the bus bar structure, $\boldsymbol{C_{BUS}}$. That coefficient depends on damping factor of the equivalent $\boldsymbol{LC}$ circuit and ratio between falling time and resonant frequency of the bus inductance and the bus stray capacitance $\boldsymbol{C_{BUS}}$.

To keep the total collector emitter voltage into the device specification, the commutation current rate must satisfy the condition (7).

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$$\left|\frac{dI_C}{dt}\right| < \frac{V_{CES} - V_{BUS\max} - V_{DFDY\max}}{(L_{BUS} + ESL_E + L_{CE})k_S}. \quad (7)$$

The voltage V_{CES} is maximum collector emitter voltage defined in the date sheet of the IGBT, for conditions V_{GE}=0 and T_{CASE}=25 °C. The V_{BUSmax} is maximum of the dc bus voltage which depends on the converter application.

Conventional driving methods - principle and the disadvantages

A conventional IGBT control is based on a simple gate driver whose block diagram is depicted in Fig. 4. The gate driver consists of a gate resistor which is usually split in two resistors R_{G_ON} and R_{G_OFF}, low impedance output buffers, a digital control unit which drives the buffers, and the gate driver power supply V_{CC}, usually 15 V, and V_{EE}, usually -5 to -15 V The gate resistors are utilized to limit the gate current and to adjust switching speed of the IGBT. In addition, the gate driver employs a short circuit detection based on monitoring of the collector emitter voltage and detection of the IGBT de-saturation in case of extensive collector current. In order to limit the turn off over-voltage, the IGBT is switched off via a large gate resistor R_{G_ERROR}. The gate emitter voltage declines slowly and the IGBT switches off without significant over-voltage. This solution is widely used in conventional gate drivers. There are, however, a few situations in which the soft turn off circuit does not work properly. In such situations we do not have any control over the IGBT turn off over-voltage, and the IGBT could be destroyed easily.

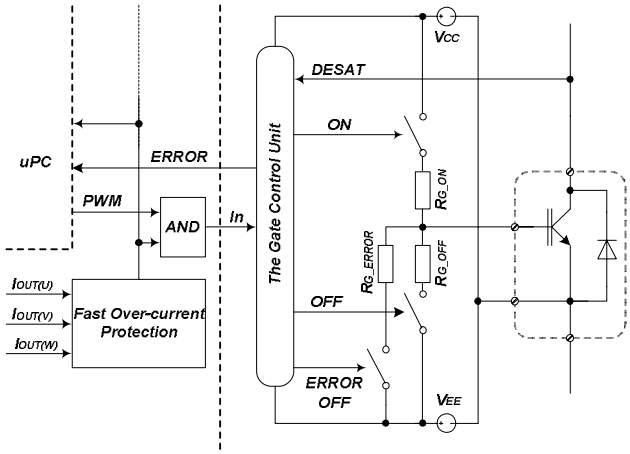

Fig. 4: A conventional gate driver circuit diagram.

The IGBT could be turned off by a command from three different signals; the PWM control signal, fast over-current protection signal, or error signal comes from the DESET short circuit detection. We can distinguish two different scenarios described in Fig. 5.

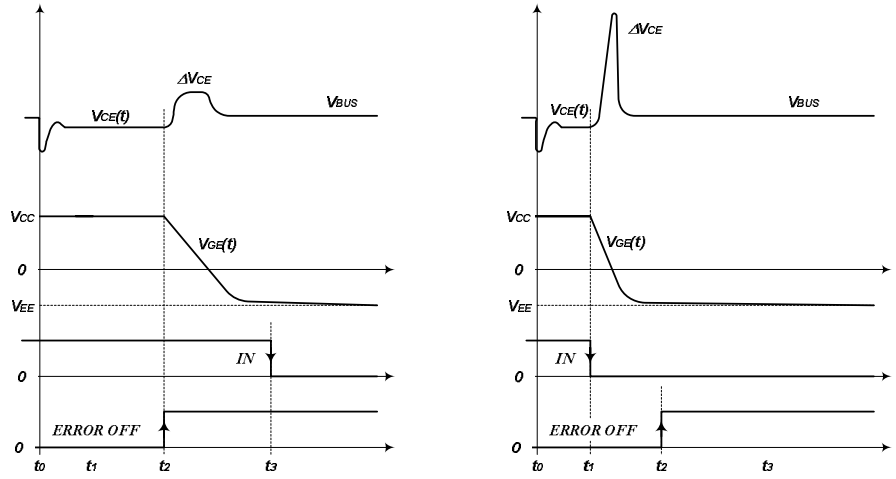

Fig. 5: The IGBT short circuit turn off scenarios.

The first scenario is described in Fig. 5a. The short circuit is detected and afterward, at the moment t_2, the IGBT is switched off softly, without any significant over-voltage. Some time after, at the instant t_3, the input command ***IN*** which comes from the PWM modulator or fast external short circuit protection

is deactivated. The IGBT has been already switched off, and the input command ***IN*** has not any effect on the IGBT state.
The second turn off scenario is described in Fig 5b. The IGBT is in short circuit. The short circuit detection and soft turn off are delayed due to the blanking time, $T_{BLT} \cong t_2$, which is necessary in order to avoid a false trip while the IGBT normally commutes. In mean time, however, the input ***IN*** command could be deactivated at the moment t_1. As we mentioned above, it could be the command from PWM modulator, or rather command from the external fast over-current protection. In such a case, the gate emitter voltage declines quickly and the IGBT turns off brutally. As a result, the short circuit current is commuted from the IGBT to the FWD quickly, causing very high over-voltage. Often, the commutation is finished by catastrophic failure of the IGBT.
Let's see how we can control over-voltage in such a situation. As we mentioned in the previous section, the IGBT is de-saturated and works in linear region. Referring to equation (5) and the equivalent circuits given in Fig. 2 and Fig. 3, the collector current rate can be estimated as:

$$\frac{dI_C}{dt}(I_{SC}) = \frac{V_{EE} - V_{GETH} - \frac{I_{SC}}{g_m}}{\frac{R_{GOFF} C_{GE}}{g_m} + L_E} \cong \frac{V_{EE} - V_{CC}}{\frac{R_{GOFF} C_{GE}}{g_m} + L_E}. \quad (8)$$

The collector current rate strongly depends on the gate resistance, gate capacitance and the IGBT trans-conductance g_m. To reduce the collector current slope and over-voltage, a large gate resistor has to be used. This approach, however, will cause significant turn off losses and turn off delay time while the IGBT normally operates. From a practical point of view this is not acceptable, and we have to find more advanced solution.

The proposed feed-forward control

In this section we will present and discuss a gate driver which solves the problem mentioned in the previous section. The solution is based on feed-forward control of the gate emitter voltage and collector current [19]. Fig. 6 shows a block diagram of the presented solution. The gate driver consists of a gate voltage shape generator, an output stage as voltage follower and a damping gate resistor R_G. The gate voltage shape generator provides a reference gate emitter voltage with approximately constant slope. This slope is adjusted according to the required slope of the gate emitter voltage and collector current respectively. The output stage in push-pull topology is a voltage follower which provides decoupling between the gate emitter voltage shape generator and the gate of the IGBT.

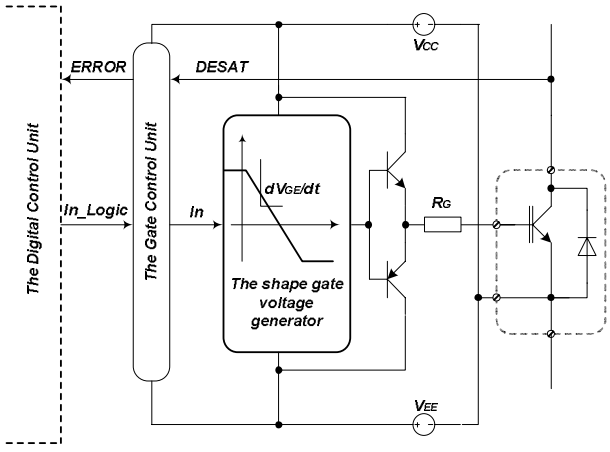

Fig. 6: The proposed feed forward gate driver circuit diagram.

The gate resistor R_G is used as a damping resistor to prevent oscillations and instability of the gate voltage due to gate inductance and the gate capacitance. The resistor R_G is selected for reasonable damping, usually ξ_{GE} =*0.7-0.9*.

$$R_G \geq 2\xi_{GE}\sqrt{\frac{L_{GE}}{C_{GE}}} \tag{9}$$

Where L_{GE}=*50-150 nH* is the total inductance in the gate circuit, including internal and external inductance, and C_{GE} is the gate emitter capacitance. Normally, the gate resistor is significantly smaller than the resistor recommended by the IGBT manufacture. Therefore, we may assume that gate circuit time constant is negligible compared to the fall time $\boldsymbol{T_{FRF}}$ of the gate voltage reference. In other words, we may assume that the $\boldsymbol{dV_{GE}/dt}$ is independent on the gate resistor $\boldsymbol{R_G}$.

$$R_G C_{GE} << T_{FRF} \cong \frac{V_{CC} + |V_{EE}|}{\frac{dV_{REF}}{dt}} \tag{10}$$

At the moment $\boldsymbol{t_0}$ the reference voltage $\boldsymbol{V_{REF}}$ begins to decline with an approximate constant slope. The gate capacitance $\boldsymbol{C_{GE}}$ is being discharged and the gate emitter voltage $\boldsymbol{V_{GE}}$ follows the reference voltage with a slight difference. The gate emitter voltage reaches the threshold voltage $\boldsymbol{V_{GE(TH)}}$ and the IGBT is turned off. Referring to the equivalent circuit in Fig 3, the quasi-steady state model given in (3) and assumption (10), the collector current can be expressed as

$$I_C \cong \left.\frac{dV_{REF}}{dt}\right|_C \cdot g_m \cdot \left(g_m L_E \left(1 - e^{-\frac{t}{g_m L_{E1}}} \right) - t \right) + I_{SC}\,, \tag{11}$$

where $\boldsymbol{I_{SC}}$ is the short circuit current has been defined in equation (5). The collector current rate is

$$\frac{dI_C}{dt} \cong g_m \left.\frac{dV_{REF}}{dt}\right|_C \cdot \left(e^{-\frac{t}{g_m L_{E1}}} - 1 \right). \tag{12}$$

The gate voltage shape generator

The key element of the proposed gate driver is a gate voltage shape generator which provides a reference gate voltage with desired slope and magnitude. Fig. 7 shows a shape generator based on passive ***RLCD*** circuit with an output buffer.

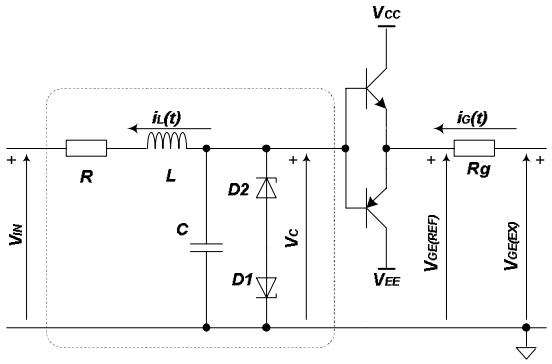

Fig. 7: The gate voltage shape generator.

The ***RLC*** circuit is slightly damped, with a damping factor of ζ=*0.2* to *0.5*. It ensures that the reference voltage has almost a constant slope in voltage range of our interest; from the $\boldsymbol{V_{CC}}$ to $\boldsymbol{V_{GE(TH)}}$. However, since the **RLC** circuit is slightly damped, the capacitor voltage $\boldsymbol{V_C}$ has tendency for overshoot of 20 to 50%. The zener diodes ***D1*** and ***D2*** are utilized to limit this voltage on level of 5 to 10 % below the supply voltage $\boldsymbol{V_{EE}}$. The input voltage $\boldsymbol{V_{IN}}$, which comes from the previous stage, equals to the positive gate supply voltage $\boldsymbol{V_{CC}}$. Thus, the capacitor $\boldsymbol{C}$ is charged also on the same voltage $\boldsymbol{V_{CC}}$. Now, we will assume that at the moment $\boldsymbol{t_0}$ the input voltage $\boldsymbol{V_{IN}}$ switches to the negative voltage $\boldsymbol{V_{EE}}$, and excites the ***RLC*** circuit. Then the voltage $\boldsymbol{V_C}$ and the reference voltage $\boldsymbol{V_{REF}}$ falls down. At the moment $\boldsymbol{t_2}$ the voltage on the capacitor $\boldsymbol{C}$ reaches the breakdown voltage of the zener diode ***D1*** and remains constant at the level $\boldsymbol{V_{ZD1}+V_{DF2}}$. The reference voltage $\boldsymbol{V_{REF}}$ follows the capacitor voltage $\boldsymbol{V_C}$ with an error of $\boldsymbol{V_{BE}\cong 0.7\ V}$.

The natural frequency ω_N of the ***RLC*** circuit for a desired slope of the reference voltage is

$$\omega_N = 1.05 \cdot \left(\frac{dV_{REF}}{dt} \right) \cdot \frac{\sqrt{1-\xi^2}\, \exp\left(\frac{\alpha\xi}{\sqrt{1-\xi^2}} \right)}{\left(V_{CC} + |V_{EE}| \right) \sin\alpha}, \tag{13}$$

where dV_{REF}/dt is desired slope of the reference gate voltage and α is angle at which the slope of the reference gate voltage is maximal. The coefficient **1.05** takes in account the fact that the reference voltage slope is not constant, but varies roughly within +/- 5% around average value (for the reference voltage V_{REF} =5 to 15 V). The angle α is calculated as

$$\alpha = arctg\left(\frac{\sqrt{1-\xi^2}}{\xi} \right). \tag{14}$$

The capacitor ***C*** is selected based on the IGBT input capacitance C_{ISS} and current gain β_{BUFFER} of the gate driver PUSH-PULL buffer. Then, the inductance and resistance of the ***RLC*** circuit are calculated based on desired natural frequency (13) and damping factor.

$$C \geq (5 \div 10)\frac{C_{ISS}}{\beta_{BUFFER}} \qquad \Rightarrow L = \frac{1}{\omega_N^2 C} \qquad \Rightarrow R = 2\xi\sqrt{\frac{L}{C}} \tag{15}$$

Experimental Results

Experimental results are presented for two IGBT modules under hard-switched conditions. The experimental set up is based on a step-down converter whose circuit diagram is depicted in Fig. 8, which represents one phase of a hard-switched PWM inverter. The IGBT modules used in the experiments are a 400 A 600 V dual module and 200 A 600 V six pack module. The collector emitter voltage was measured between auxiliary emitter of the lower device and output terminal. We can suppose that voltage measured between these two points is reasonable close to the voltage across the collector to base junction of the internal PNP BJT. The voltage was measured with a calibrated passive high-voltage probe, with bandwidth of 400 MHz. The short circuit current was measured with a Rogowski Current Transducer CTW30.

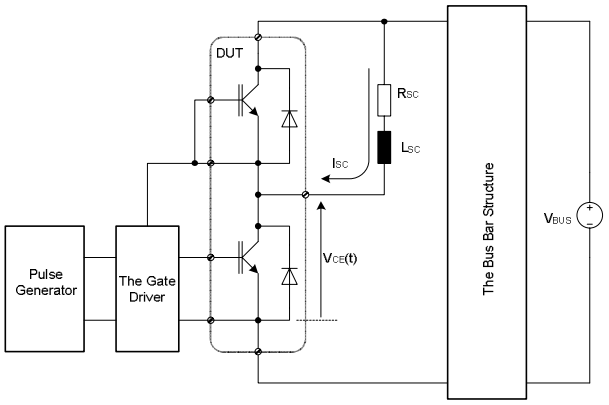

Fig. 8: The experimental set up.

For the safety reasons, the tests with a conventional gate driver have been done at the dc bus voltage of 300V, while the tests with the proposed gate driver have been done with the full dc bus voltage of 405V. Fig. 9 presents results of short circuit test of 400A 600V IGBT dual module in NPT technology. The waveforms depicted in Fig. 9a were recorded on the IGBT driven by a standard gate driver with the recommended value of the gate resistor. Fig. 9b shows waveforms of the IGBT driven by the proposed feed-forward gate driver. The over-shoot with the IGBT driven by the standard gate driver is ΔV_{CE}=280V compared to the over-shoot of ΔV_{CE}=66V with the proposed gate driver.

The test results of a six-pack 200 A IGBT module are presented in Fig. 10. The waveforms of the IGBT driven by a conventional gate driver are depicted in Fig. 10a. The collector emitter over-shoot is ΔV_{CE}=270V. We can observe high frequency oscillations in the final stage of the commutation. In contrast to this, the waveforms of the IGBT driven by the propose gate driver are clean, without any high frequency oscillations. The collector emitter over-voltage is ΔV_{CE}=36V.

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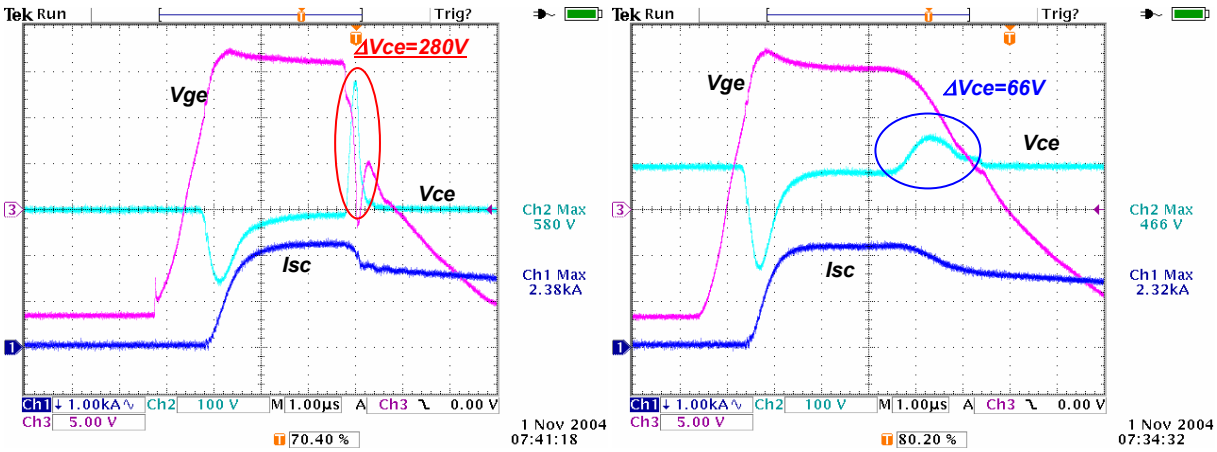
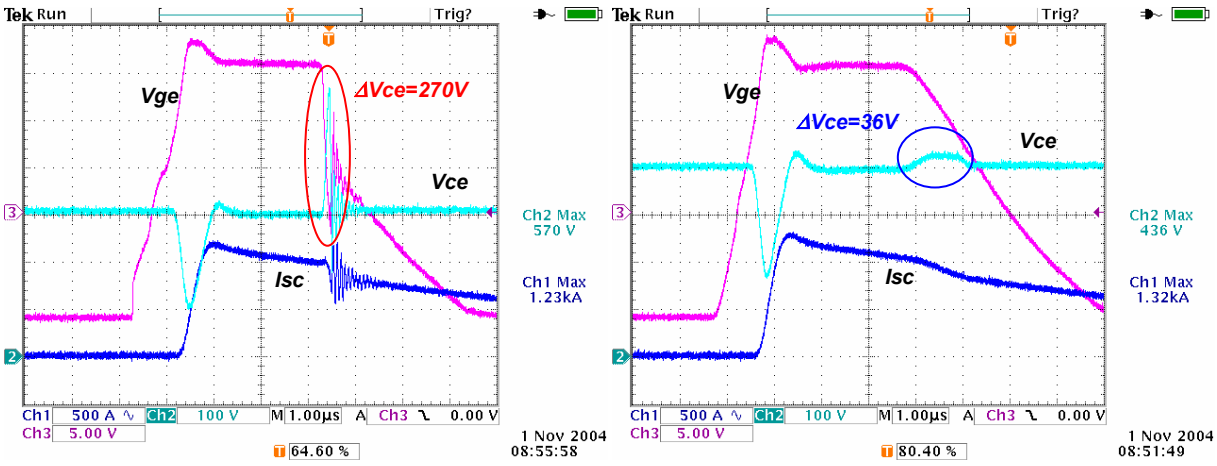


a) b)

Fig. 9: The collector emitter voltage, gate emitter voltage and short circuit current; 400A IGBT driven by a standard gate driver (a), and the feed-forward gate driver (b).



a) b)

Fig. 10: The collector emitter voltage, gate emitter voltage and short circuit current; 200A IGBT module driven by a standard gate driver (a) and the feed-forward gate driver (b).

Conclusions

This paper presented a feed-forward control of an IGBT over-voltage generated during a short circuit switch of. The IGBT turn off characteristic and possibility to control over voltage using a feed forward gate driver has been shortly presented. The experimental measurements have been performed on two different IGBT modules, and the results were presented in this paper. The tests with a conventional gate driver have been done at nominal dc bus voltage of 300V, while the tests with the proposed gate driver have been done at the maximum dc bus voltage of 405V.

The collector emitter over-voltage measured with a conventional gate driver was 280V. In case of the maximum bus voltage of 405V, the total collector emitter voltage will be above breakdown level. The IGBT will go to avalanche and catastrophically failed. In contrast to that, the IGBT driven with the proposed feed-forward gate driver safely switches off short circuit current in all possible operational conditions including the highest bus voltage of above 400V. The proposed gate driver provides simple and robust control of the collector emitter over-voltage in all possible short circuit turn off scenarios.

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